

DC/DC Module Trim with Digital Potentiometers

Introduction

This Application Note describes the trimming technique for DC/DC converter modules using industry standards for output voltage trim. The DC/DC converter module design equations are presented from the datasheets, a circuit model for the DC/DC converter is shown, circuit equations for using a digital pot (DCP) are derived and resistor values are shown for the two most popular industry standards.

As of this writing, there are two standards for DC/DC converter module that attempt to create standard pinouts, standard package size, standard electrical specifications and standard controls such as ON/OFF and output voltage setting.

The first standard was the Point of Load Alliance (POLA) established by Texas Instruments, Artyzen, Emerson Astec, Ericsson and others. A typical POLA DC/DC converter module is the Texas Instruments PTH12050, which features an adjustable output voltage of 0.8V to 5.5V with a 6 amp output current from a +12V input voltage. There are many other variations of this DC/DC converter module for other input voltages and load currents from any vendor that is part of the POLA. Within their product families, all POLA modules are interchangeable and, therefore, second sourced by any POLA vendor. Appendix A on [page 5](#) shows the typical voltage setting technique and datasheet trim circuit.

The second standard that is more recent is the Distributed Power Open Standards Alliance (DOSA) founded by Tyco Electronics and SynQor; recent members include Celestica, Delta, Ericsson and Lambda. Their web site is www.dosapower.com for additional information. A typical DOSA DC/DC converter module is the Tyco Electronics Austin Lynx II # ATA010A0X3-SR which features an adjustable output voltage of 0.75V to 5.0V with a 10 amp output current from a +12V input voltage. There are many other variations of this DC/DC converter module for other input voltages and load currents from any vendor that is part of the DOSA. Within their product families, all DOSA modules are interchangeable and, therefore, second sourced by any DOSA vendor. Appendix B on [page 5](#) shows the typical voltage setting technique and datasheet trim circuit. Throughout this application note, the Texas Instruments PTH12050 POLA module and Tyco Austin Lynx II # ATA010A0X3-SR DOSA module are shown in the design examples. However, any module which complies with the POLA or DOSA standard should be interchangeable.

It must be noted that POLA modules are not pin compatible with DOSA modules. Also, DC/DC converter modules, which are not part of POLA or DOSA may or may not be compatible with DC/DC converter modules from other vendors.

Module trim with software control of a DC/DC converter module output voltage is desirable for several reasons:

1. Margin testing is often required in the engineering qualification test to four-corner test the system against tolerance variations in the DC/DC converter output voltages.
2. Margin testing is often performed as part of production final system tests.
3. Margin testing can be done as part of a regular in-field preventative maintenance test to attempt to predict a system failure.
4. As the core voltage requirement of controllers, gate arrays, etc. change with each new generation of devices it is helpful to be able to perform software changes of output voltage instead of requiring an ECO to change a resistor value.

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POLA Modules DCP Circuit and Table of Resistors Values

Figure 1 and Tables 1 and 2 show the circuit for interfacing POLA modules to a DCP. For high output voltage (1.2V to 5.5V) POLA modules (PTH12050W) the circuit and tables show the external resistor values (R_W , R_Y) for an ISL95810UIU8 256 tap, 50k DCP. The ISL95810UIU8 DCP allows an adjustment range of nominal $V_{OUT} \pm 10\%$ by changing the DCP code from full scale value (255_{10}) to zero value (000_{10}). The complete circuit analysis, circuit model and design equations are shown in Appendix C on page 6 and Appendix D on page 7.

For low output voltage (0.8 to 1.8V) POLA modules (PTH12050L) Table 2 shows the external resistor values (R_W , R_Y) for an ISL95810UIU8 256 tap, 50k DCP.

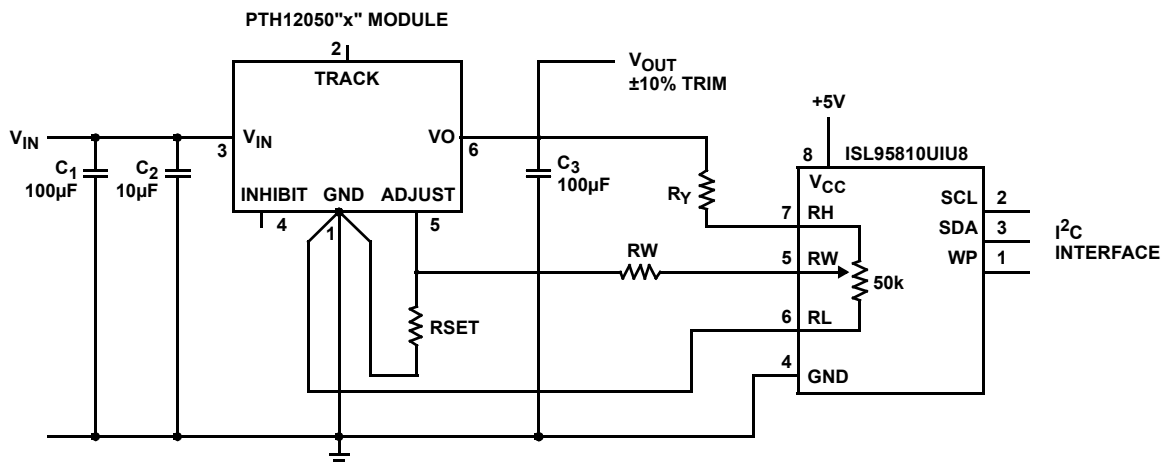
TABLE 1. HIGH OUTPUT VOLTAGE RESISTOR VALUES FOR POLA MODULE

NOMINAL V_{OUT} (VDC)	MINIMUM V_{OUT} (VDC)	MAXIMUM V_{OUT} (VDC)	R_{SET} (k Ω)	R_W (k Ω)	R_Y (Ω)
3.3	3.000	3.600	1.69	14.3	8.06k
2.5	2.250	2.750	3.83	26.1	2.49k
1.8	1.620	1.980	11	36.5	511
1.5	1.372	1.651	26.7	39.2	0

Minimum V_{OUT} at Full Scale Code
 Nominal V_{OUT} at 1/2 Full Scale Code
 Maximum V_{OUT} at Zero Code

TABLE 2. LOW OUTPUT VOLTAGE RESISTOR VALUES FOR POLA MODULE

NOMINAL V_{OUT} (VDC)	MINIMUM V_{OUT} (VDC)	MAXIMUM V_{OUT} (VDC)	R_{SET} (k Ω)	R_W (k Ω)	R_Y (Ω)
1.5	1.350	1.650	2.61	3.74	6.65k
1.2	1.080	1.320	11.5	21.5	422
1.0	0.900	1.100	44.2	32.4	0



"x" indicates W-suffix for 1.2V to 5.5V Module.
 "x" indicates L-suffix for 0.8V to 1.8V Module.

FIGURE 1. CIRCUIT FOR POLA MODULE

DOSA Modules DCP Circuit and Table of Resistors Values

For DOSA modules (Tyco Austin Lynx II, # ATA010A0X3-SR) [Figure 2](#) and [Table 3](#) show the external resistor values (R_W , R_Y) for an ISL95810UIU8 256 tap, 50k DCP. The ISL95810UIU8 DCP allows an adjustment range of nominal $V_{OUT} \pm 10\%$ by changing the DCP code from full scale value (255_{10}) to zero value (000_{10}). The complete circuit analysis, circuit model and design equations are shown in Appendix C on [page 6](#) and Appendix E on [page 8](#).

TABLE 3. RESISTOR VALUES FOR DOSA MODULE

NOMINAL V_{OUT} (VDC)	MINIMUM V_{OUT} (VDC)	MAXIMUM V_{OUT} (VDC)	R_{TRIM} (k Ω)	R_W (k Ω)	R_Y (Ω)
5.0	4.500	5.500	1.27	26.1	7.87k
3.3	3.000	3.600	2.87	47.5	4.32k
2.5	2.250	2.750	4.64	51.1	1.96k
1.8	1.620	1.980	8.66	59	309
1.5	1.372	1.651	12.7	68.1	0
1.2	1.080	1.320	23.7	66.5	0

Minimum V_{OUT} at Full Scale Code
 Nominal V_{OUT} at 1/2 Full Scale Code
 Maximum V_{OUT} at Zero Code

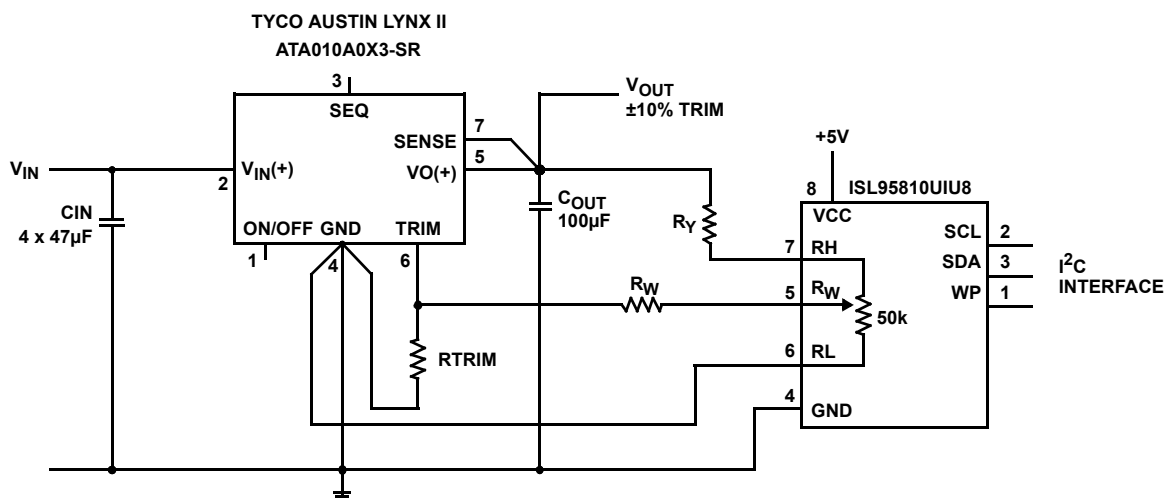


FIGURE 2. CIRCUIT FOR DOSA MODULE

Example of Vicor DC/DC Converter Modules

For Vicor Generation 2 modules (#V48C5C100B for example) [Figure 3](#) and [Table 4](#) show the external resistor values (R_W , R_Y) for an ISL95810UIU8 256 tap, 50k DCP. The ISL95810UIU8 DCP allows an adjustment range of nominal $V_{OUT} \pm 10\%$ by changing the DCP code from full scale value (255_{10}) to zero value (000_{10}). The complete circuit analysis, circuit model and design equations are shown in Appendix F on [page 8](#).

TABLE 4. RESISTOR VALUES FOR VICOR GENERATION 2 MODULE

NOMINAL V_{OUT} (VDC)	MINIMUM V_{OUT} (VDC)	MAXIMUM V_{OUT} (VDC)	Rpot End-End (k Ω)	R_W (k Ω)	R_Y (k Ω)
5.0	4.500	5.500	50	9.09	17.4

Discrete DC/DC Converter Circuits Using Intersil Monolithic 2A Step-Down Regulator IC

The same technique for using a DCP to trim the output voltage of a DC/DC converter module can also be applied to a discrete DC/DC converter circuit as shown in [Figure 4](#). The EL7532 circuit is set for a nominal output voltage of 1.8V. The ISL95810UIU8 DCP allows an adjustment range of 1.62V to 2.00V ($1.8V \pm 10\%$) by changing the DCP code from full scale value (255_{10}) to zero value (000_{10}). The circuit analysis for the output voltage vs code is similar to the analysis for the POLA or DOSA module as described in the Appendix C on [page 6](#) and is available upon request.

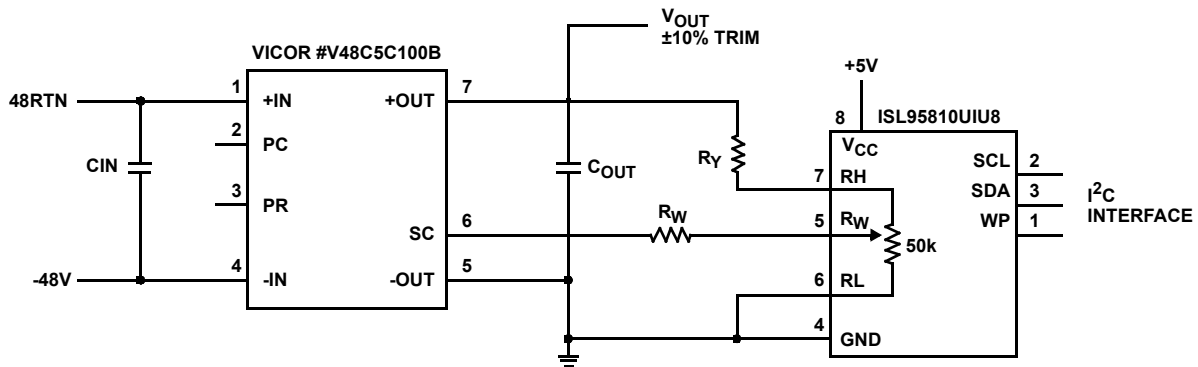


FIGURE 3. CIRCUIT FOR VICOR GENERATION 2 MODULE

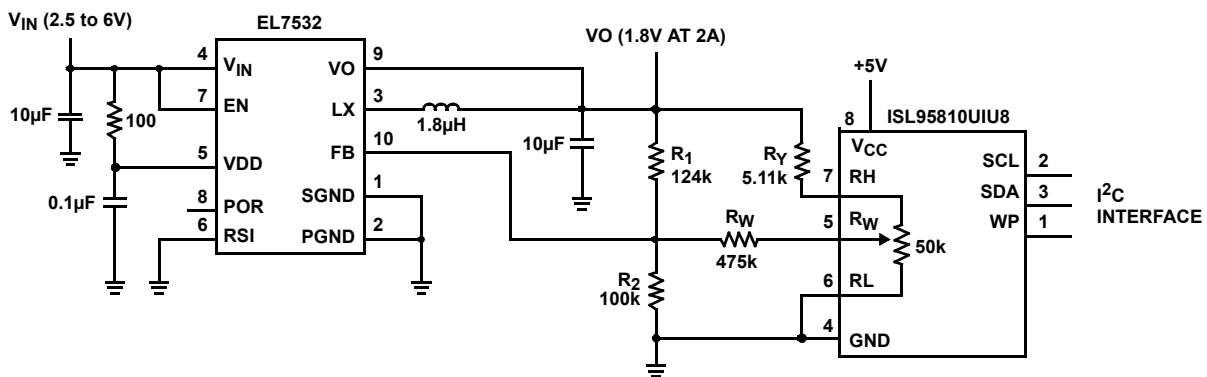


FIGURE 4. CIRCUIT FOR DISCRETE DC/DC MODULE

Appendix A: Standard POLA Output Voltage Settings and Trim

To set the output voltage of a POLA DC/DC converter module, an external resistor, R_{SET} , is added from the Adjust pin to the GND pin as shown in [Figure 5](#). With the TI #PTH12050 DC/DC converter module there are two parts - one for high output voltage (1.2V to 5.5V) indicated by a W suffix and a second for low voltage (0.8V to 1.8V) indicated by an L suffix.

$$R_{SET} = 10k / (V_o - V_{MIN}) - R_s$$

Where V_o = Desired output voltage

V_{MIN} = 1.2V for W-suffix part

= 0.8V for L-suffix parts

R_s = 1.82k Ω for W-suffix parts

= 7.87k Ω for L-suffix parts

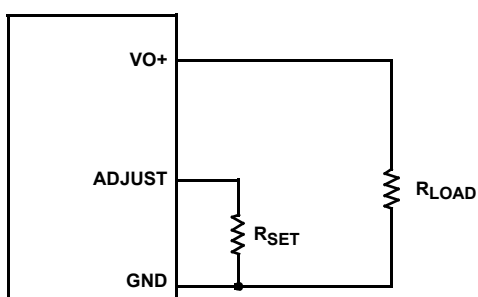


FIGURE 5. POLA OUTPUT VOLTAGE SET CIRCUIT

Output voltage margining is implemented by adding external resistors for margining up ($R_{MARGIN-UP}$) and margining down ($R_{MARGIN-DOWN}$); the resistors are connected into the Trim pin with external N-channel FETs Q1 and Q2. With this technique only three output voltages can be set; nominal (both Q1 and Q2 off), margin up output voltage (Q1 on) and margin down voltage (Q2 on). No intermediate voltage steps are available.

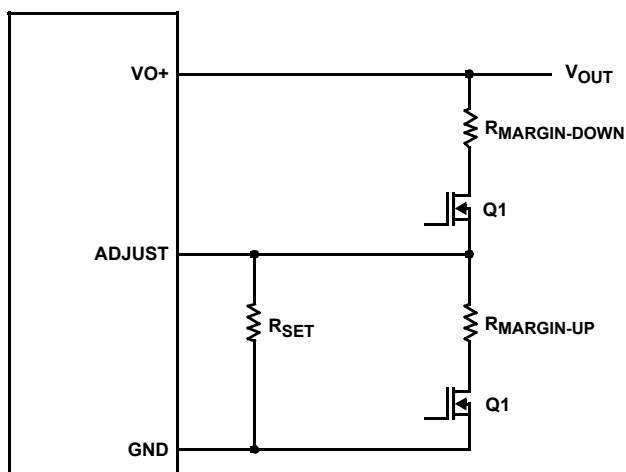


FIGURE 6. POLA MARGIN CIRCUIT

Other POLA modules (PTH12060W) include Margin Up and Margin Down pins for $\pm 5\%$ output voltage margining. However, they require external FETs for controlling the Margin Up and Margin Down pins.

Replacing the two resistors and FETs with a digital pot (DCP) allows a large number of output voltages to be set under software control. It will be shown in the next section that the range of the output voltage can be set with two fixed resistors connected to the DCP wiper and top terminal.

Appendix B: Standard DOSA Output Voltage Settings and Trim

To set the output voltage of a DOSA DC/DC converter module, an external resistor, R_{TRIM} is added from the TRIM pin to the GND pin as shown in [Figure 7](#).

$$R_{TRIM} = 10500 / (V_o - 0.7525) - 1000$$

Where V_o = Desired output voltage

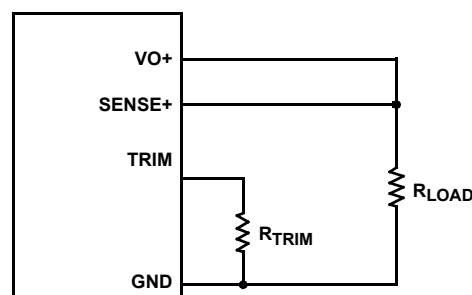


FIGURE 7. DOSA OUTPUT VOLTAGE SET CIRCUIT

Output voltage margining is implemented by adding external resistors for margining up ($R_{MARGIN-UP}$) and margining down ($R_{MARGIN-DOWN}$); the resistors are connected into the Trim pin with external N-channel FETs Q1 and Q2. With this technique only three output voltages can be set; nominal (both Q1 and Q2 off), margin-up output voltage (Q1 on) and margin-down voltage (Q2 on). No intermediate voltage steps are available.

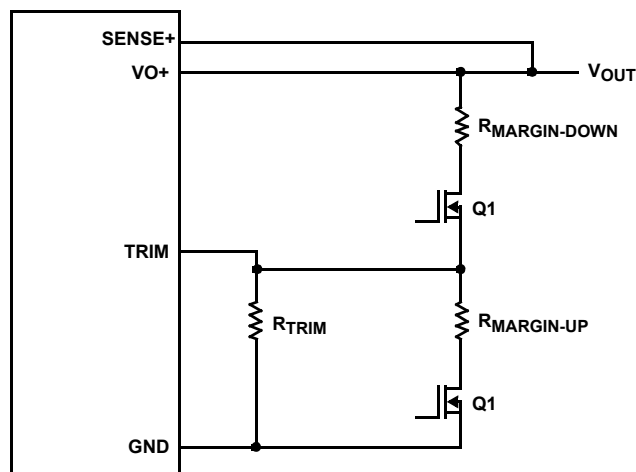


FIGURE 8. DOSA MARGIN CIRCUIT

Replacing the two resistors and FETs with a DCP allows a large number of output voltages to be set under software control. It will be shown in the next section that the range of the output voltage can be set with two fixed resistors connected to the DCP wiper and top terminal.

Appendix C: POLA and DOSA DC/DC Converter Circuit Model and Design Equations

To use a DCP for controlling the output voltage of a DC/DC converter module it is necessary to obtain a circuit model of the feedback circuit internal to the DC/DC converter module. Some DC/DC converter module vendors show the circuit model on their datasheets or application notes. If the circuit model is not available, it is necessary to derive the model from the output voltage vs adjust resistor equation.

The output voltage of a POLA or DOSA DC/DC converter module can be adjusted for trimming and margining purposes by using the circuit in [Figure 9](#). Resistor R_W sets the width of the adjustment range and resistor R_Y is used to center the adjustment range around its nominal output with the DCP set to midscale. Because the DCP presents a "load" to the feedback network, the resistance of both sides of the DCP must be considered.

For analysis, the equivalent circuit with node assignments is used ([Figure 10](#)).

Summing Currents at Each Node:

$$(V_o - V_r)/R_1 + (V_1 - V_r)/R_S + (0 - V_r)/R_2 = 0 \quad (\text{Node } V_r)$$

$$(V_r - V_1)/R_S + (V_2 - V_1)/R_W + (0 - V_1) R_{ADJ} = 0 \quad (\text{Node } V_1)$$

$$(V_o - V_2)/R_T + (V_1 - V_2)/R_W + (0 - V_2)/R_B = 0 \quad (\text{Node } V_2)$$

For a DCP

$$R_{BOT} = R_{EE} * \text{Code}/N$$

$$R_{TOP} = R_{EE} - R_{BOT}$$

Where R_{EE} = DCP end to end resistance

Code = Digital input code (0 to N)

N = Number of taps

Solving for V_o :

$$V_o = V_r * (X - R_1/(B * D * R_s^2)) / (1 + E * R_1/R_S)$$

$$\text{Where } X = 1 + R_1/R_S + R_1/R_2$$

$$B = 1/R_S + 1/R_W + 1/R_{ADJ}$$

$$C = 1/R_T + 1/R_W + 1/R_B$$

$$D = 1 - 1/(B * C * R_W^2)$$

$$E = 1/(B * C * D * R_W * R_T)$$

$$R_T = R_{TOP} + R_Y$$

Since this is a very messy non-linear equation, an [Excel worksheet](#) was prepared to calculate the DC/DC converter module output voltage with a given DCP digital code.

In addition to the Excel worksheet, to calculate the output voltage with a DCP code, R_W and R_Y resistor values, the three node equations were programmed into TK Solver (Universal Technical Systems). TK Solver has the ability to back solve a set of equations with any variable being set as an input or output variable. The TK Solver rules sheet is available upon request.

A SPICE simulation could also be used to calculate the output voltage with a DCP input code; however, SPICE does not provide the ability to calculate resistor values. SPICE could only be used to verify the circuit analysis and calculate the output voltage with a DCP input code

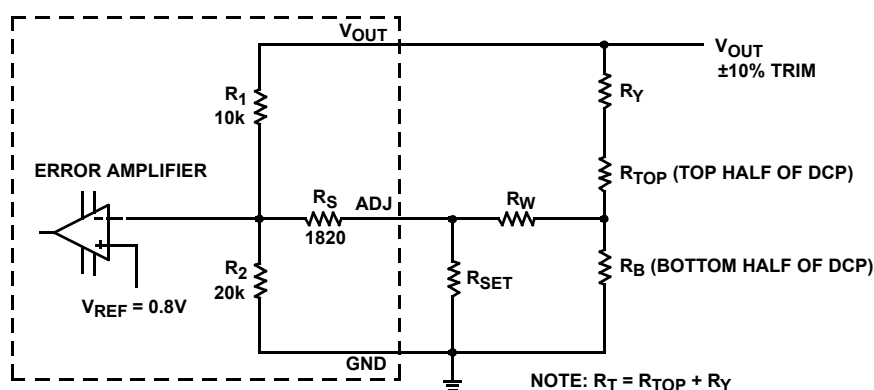


FIGURE 9. POLA MODULE CIRCUIT MODEL WITH DCP

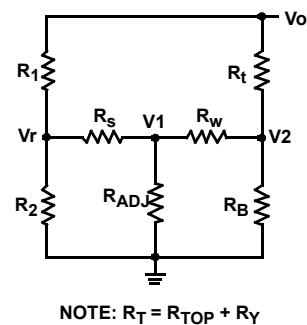


FIGURE 10. EQUIVALENT POLA MODULE CIRCUIT WITH NODE ASSIGNMENT

Appendix D: POLA DC/DC Converter Circuit Model

The POLA DC/DC converter module circuit model high output voltage parts is shown in [Figure 11](#).

For low output voltage (0.8V to 1.8V) POLA DC/DC converter module, resistor R_2 (20k) is removed and R_S value is changed to 7.87k; the circuit model is shown in [Figure 12](#).

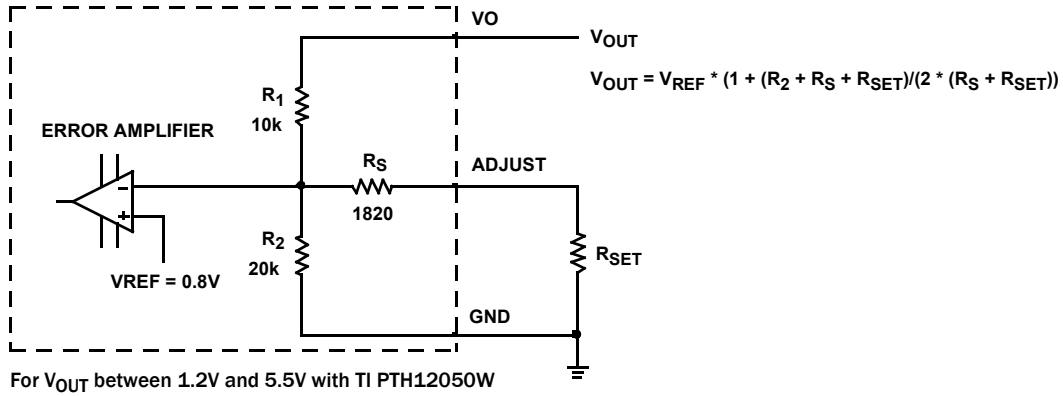


FIGURE 11. HIGH OUTPUT VOLTAGE POLA MODULE CIRCUIT MODEL WITH DCP

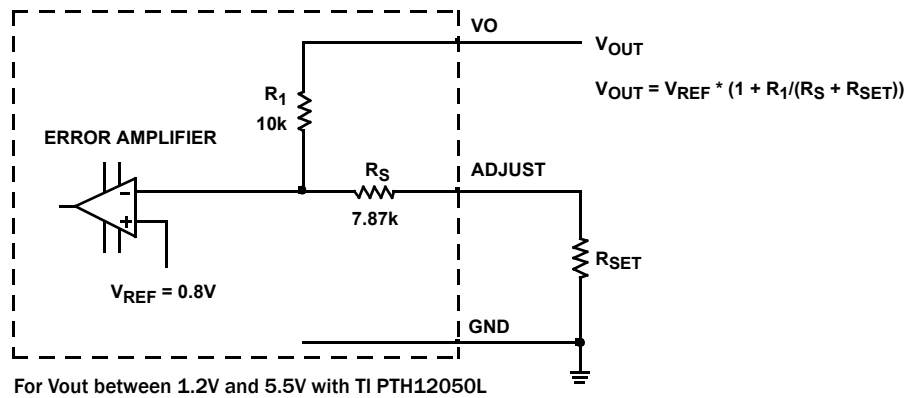


FIGURE 12. LOW OUTPUT VOLTAGE POLA MODULE CIRCUIT MODEL WITH DCP

Appendix E: DOSA DC/DC Converter Circuit Model

The circuit model for a DOSA DC/DC converter module is very similar to the POLA modules as shown in [Figure 13](#).

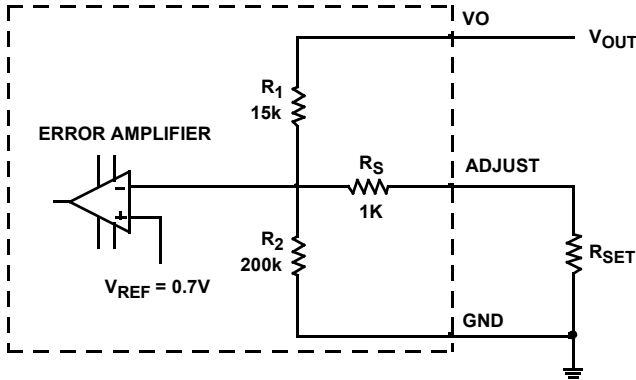


FIGURE 13. DOSA MODULE CIRCUIT MODEL WITH DCP

Appendix F: Vicor Generation 2 DC/DC Converter Circuit Model and Design Equations

The output voltage of a Vicor Generation 2 DC/DC converter module can be adjusted for trimming and margining purposes by using the circuit shown in [Figure 14](#). Resistor R_W sets the width of the adjustment range and resistor R_Y is used to center the adjustment range around its nominal output with the DCP

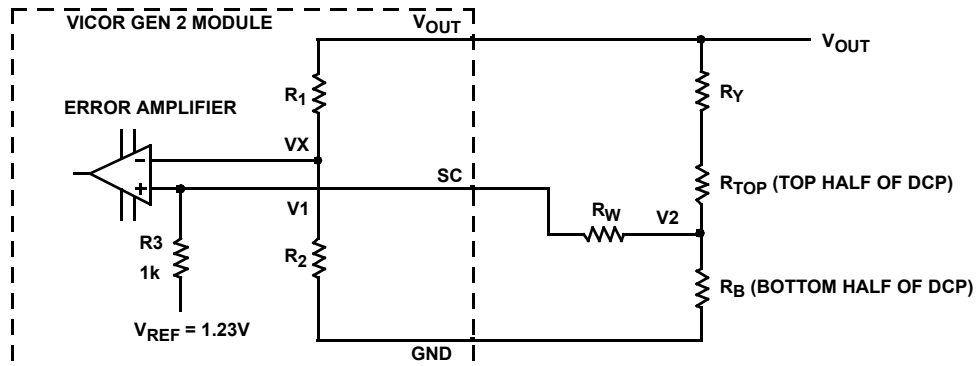


FIGURE 14. VICOR GENERATION 2 MODULE CIRCUIT MODEL WITH DCP

set to midscale. Because the DCP presents a “load” to the feedback network, the resistance of both sides of the DCP must be considered. For analysis, the equivalent circuit with node assignments is used in [Figure 14](#).

Summing Currents at V1 and V2 Node:

$$(V_{REF} - V1)/R_3 + (V2 - V1)/R_W = 0 \quad \text{Node V1}$$

$$(V1 - V2)/R_W + (V_{OUT} - V2)/(R_Y + R_{TOP}) + (0 - V2)/R_{bot} = 0 \quad \text{Node V2}$$

The error amplifier will force $V1 = Vx$

Resistors R_1 and R_2 are not shown on the datasheet or application notes; however, it is easy to determine the ratio R_1/R_2 based on circuit analysis when there is no trim applied.

With no trim applied to the SC pin

$$V_{nom} = V_{REF} * (1 + R_1/R_2) \quad \text{where } V_{nom} \text{ is the output voltage with no trim.}$$

$$R_1/R_2 = V_{nom}/V_{REF} - 1$$

Summing Currents at Vx Node

$$(V_{OUT} - Vx)/R_1 + (0 - Vx)/R_2 = 0$$

$$V_{OUT} = Vx * (1 + R_1/R_2)$$

Plugging R_1/R_2 from the No Trim Calculation

$$V_{OUT} = Vx * V_{nom}/V_{REF}$$

To calculate the output voltage with a DCP code, R_W and R_Y resistor values, the two node equations, $V1 = Vx$ and $V_{OUT} = Vx * V_{nom}/V_{REF}$ were programmed into TK Solver. The TK Solver rules sheet is available upon request.

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the document is current before proceeding.

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